Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1.A method for establishing a Gray code count sequence having N code words comprising:

determining a first bit switch sequence having 2^M-1 elements and abit switching sequence property according to a first Gray code count sequence having 2^M code words, wherein 2^M is larger than N;

determining a second bit switch sequence having N-1 elements and the bit switching sequence property according to the first bit switch sequence; and

determining a second Gray code count sequence according to the second bit switch sequence.

[c2] 2.The method of claim 1, wherein if the first bit switch sequence and the second bit switch sequence are regarded as ordered sets according to thebit switching sequence property, each ordered sub-set being of even number in the set will contain at least one numberwhich appears an odd number of times.

[c3] 3.The method of claim 1, wherein the second bit switch sequence is determined by deleting 2^M-N elements from the first bit switch sequence.

[c4] 4.The method of claim 3, wherein the first bit switch sequence further comprises a first ordered sub-set composed of the first element to the $(2^M-2)/2^{th}$ element, and a second ordered sub-set composed of the $2^M/2^{th}$ element to the 2^M-1^{th} element.

[c5] 5.The method of claim 4, wherein when deleting 2^M-N elements from the first bit switch sequence, if N is even, deleting$(2^M-N)/2$ elements from the first ordered sub-set and the second ordered sub-set respectively, in order to obtain the second bit switch sequence, wherein the deleted elements of the first ordered sub-set correspond to the deleted elements of the second ordered sub-set.

[c6] 6.The method of claim 5, wherein the values of the deleted elements of the first ordered sub-set are the same as the values of the deleted elements of the second ordered sub-set.

[c7] 7.The method of claim 5, wherein the positions of the deleted elements of the first ordered sub-set are the same as the positions of the deleted elements of the second ordered sub-set.

[c8] 8.The method of claim 5, wherein if the deleted element of the first ordered sub-set is the d^{th} element of the first

bit switch sequence, the deleted elements of the second ordered sub-set are the 2^M-d^{th} elements of the first bit switch sequence.

[c9] 9.The method of claim 5, wherein if N is odd, the step of deleting 2^M-N elements from the first bit switch sequence further comprises:
deleting (2^M-N-1)/2 first deleted elements from the first ordered sub-set and the second ordered sub-set respectively, the first deleted elements of the first ordered sub-set corresponding to the first deleted elements of the second ordered sub-set respectively; and
deleting a second deleted element to obtain the second bit switch sequence.

[c10] 10.The method of claim 9, wherein the values of the first deleted elements of the first ordered sub-set are the same as the values of the first deleted elements of the second ordered sub-set.

[c11] 11.The method of claim 9, wherein the positions of the first deleted elements of the first ordered sub-set are the same as the positions of the first deleted elements of the second ordered sub-set.

[c12] 12.The method of claim 9, wherein if the first deleted element of the first ordered sub-set is the d^{th} element of

the first bit switch sequence, the first deleted elements of the second ordered sub-set are the 2^M-d^{th} elements of the first bit switch sequence.

[c13] 13.The method of claim 9, wherein the first element and the 2^M-1^{th} element of the first bit switch sequence are the deleted elements.

[c14] 14.A Gray code counter for outputting a code word comprising:
a clock generator for outputting a clock signal; and
a first bit unit comprising:
an XOR gate for receiving a first input signal;
an AND gate for receiving a reverse second input signal and outputting a first output signal;
an OR gate for receiving a second input signal and outputting a second output signal; and
a flip flop having a signal input coupled with an output of the XOR gate, and a signal output coupled respectively with inputs of the XOR gate, the AND gate and the OR gate for outputting a bit output signal according to the clock signal,
wherein the Gray code counter is composed of a plurality of the first bit units connected serially, and the code word comprises the bit output signal.

[c15] 15.A Gray code counter comprising:

a clock generator for outputting a clock signal; and

a first bit unit comprising:

an XOR gate for receiving a first input signal;

an AND gate for receiving a reverse second input signal and outputting a first output signal;

an OR gate for receiving a second input signal and outputting a second output signal;

a flip flop having a signal input coupled with an output of the XOR gate, and a signal output coupled respectively with input of the AND gate and the OR gate, for outputting a Gray code bit output signal according to the clock signal; and

a second bit unit comprising:

an XOR gate for receiving a third input signal;

an AND gate for receiving a reverse fourth input signal and outputting a third output signal;

an OR gate for receiving a fourth input signal and outputting a fourth output signal;

a flip flop having a signal input coupled with an output of the XOR gate, and a signal output, for outputting a Gray code bit output signal according to the clock signal; and

an XNOR gate having an output connected to input ends of the AND gate and the OR gate respectively, for receiving a fifth input signal and the Gray code bit output signal,

wherein the Gray code counter is composed of the first bit unit and the second bit unit connected serially.